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CLAIMS

1. A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer;

a polysilicon layer formed on said oxide layer;

a gate structure formed from said polysilicon layer, said gate structure having a defined leading edge; and

an overlap region beneath said gate structure and adjacent said leading edge having a predetermined ion implant concentration, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

2. The circuit structure according to claim 1, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

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3. A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, the portion of said gate oxide layer which is beneath said gate electrode and adjacent said drain region, and which defines an overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said overlap region.

4. The circuit structure according to claim 3, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

5. The circuit structure according to claim 3, wherein said source region and said drain region are heavily doped with a second conductivity dopant.

6. The circuit structure according to claim 3, further including a pair of spaces adjacent said gate electrode.

7. The circuit structure according to claim 3, wherein said gate electrode is comprised of polysilicon.

8. The circuit structure according to claim 3, wherein said gate electrode is a gate stack.

9. The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

10. The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium layer.

11. The circuit structure according to claim 3, further including a pair of conductive studs and an interlevel dielectric layer provided on said semiconductive layer, said interlevel dielectric layer have a pair of throughbores, each accommodating one of each said pair of conductive studs, and one of each said pair of conductive studs contacting one of each said source/drain regions.

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12. A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, the portion of said gate oxide layer which is beneath said gate electrode and adjacent said drain region, and which defines an overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

13. The circuit structure according to claim 12, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

14. The circuit structure according to claim 12, wherein the portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.

15. A method for fabricating a structure on a semiconductor layer comprising the steps of :

forming an oxide layer on a semiconductor layer;

forming a polysilicon layer on said oxide layer;

patterning said polysilicon layer into a gate structure having a defined leading edge, and to expose said oxide layer; and

implanting ions into said oxide layer at an overlap region beneath said gate structure and adjacent said defined leading edge to a predetermined ion implant concentration, which is sufficient to increase the electrical gate oxide thickness only in said overlap region without thickness growth of said oxide layer, said ions are implanted at a tilt angle non-orthogonal to the plane of said semiconductor layer.

16. A method according to claim 15, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

17. A method according to claim 15, wherein the tilt angle is from about 5 to about 15 degrees from an axis orthogonal to the plane of the semiconductor layer.

18. A method according to claim 15, wherein said ion is selected from the group consisting of fluorine and chlorine.

19. A method according to claim 15, wherein said ion is fluorine and said implanting step is carried out at an ion implantation dose of from about 1E13 to about 1E14 atoms per square centimeter, and an ion implantation energy of from about 10 KeV to about 20 KeV.

20. A method according to claim 15, further including the step of annealing said semiconductor layer at a temperature of about 800 to about 900 degrees centigrade for a time period of about 10 to about 15 minutes.

21. A method according to claim 15, wherein said oxide layer thickness is about 20 to about 80 angstroms.

22. A method according to claim 15, further comprising forming electrode spacers on both sides of said gate structure.

23. A method according to claim 15, wherein said gate structure is comprised of polysilicon.

24. A method according to claim 15, wherein said gate structure is a gate stack.

25. A method according to claim 24, wherein said gate stack is comprised of a layer of polysilicon, and additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

26. A method according to claim 15, wherein said gate structure is a gate electrode comprised of a layer of polysilicon, a layer of titanium nitride deposited on top of said polysilicon layer, and a layer of tungsten deposited on top of said titanium layer.

27. A method according to claim 15, wherein said oxide layer is formed by low pressure chemical vapor deposition to a thickness of between about 20 to about 80 Angstroms.

28. A method according to claim 15, further comprising forming a lightly doped drain source/drain region structure within the semiconductor layer adjoining said gate structure.

29. A method according to claim 28, wherein said lightly doped regions are n-type regions formed by implanting ions, selected from the group consisting of phosphorus and arsenic, with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 5 to about 15 KeV.

30. A method according to claim 28, wherein said lightly doped regions are p-type regions formed by implanting boron di-fluoride ions with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 10 to about 25 KeV.

31. A method according to claim 15, further comprising forming a heavily doped drain source/drain region structure within the semiconductor layer adjoining the gate structure.

32. A method according to claim 31, wherein said heavily doped regions are n-type regions formed by implanting ions, selected from the group consisting of phosphorus and arsenic, with a

dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 5 to about 15 KeV.

33. A method according to claim 31, wherein said heavily doped regions are p-type regions formed by implanting boron di-fluoride ions with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 10 to about 25 KeV.

34. A method according to claim 15, further comprising forming electrode spacers on both sides of said gate structure.

35. A method according to claim 34, wherein said electrode spacers have widths of between about 300 to about 700 Angstroms.

36. A method according to claim 15, wherein said step of implanting is performed before said step of forming said polysilicon layer.

37. A method according to claim 15, wherein said step of implanting is performed before said step of patterning said polysilicon layer.

38. A method of reducing Gate Induced Drain Leakage (GIDL) current within Field Effect Transistors (FETs) comprising the steps of:

forming on a semiconductor layer a field effect transistor structure comprising a gate oxide layer, a gate electrode on the gate oxide layer and two source/drain regions formed within said semiconductor layer;

annealing said semiconductor layer;

implanting ions into said gate oxide layer beneath said gate electrode and adjacent said drain region, which defines an overlap region, to a predetermined ion implant concentration which is sufficient to increase electrical gate oxide thickness only in said overlap region, said ions being implanted at a tilt angle non-orthogonal to the plane of the semiconductor layer; and

completing the fabrication of said semiconductor layer.

39. A method according to claim 38, wherein said FET formed on said semiconductor layer is a plurality of a first FET with a first dopant type and said semiconductor layer also includes a plurality of a second FET with a second dopant type, said second FET being complimentary to said first FET.

40. A method according to claim 38, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

41. A method according to claim 38, wherein the tilt angle is from about 5 to about 15 degrees from an axis orthogonal to the plane of the semiconductor layer.

42. A method according to claim 38, wherein said ion is selected from the group consisting of fluorine and chlorine.

43. A method according to claim 38, wherein said ion is fluorine and said implanting step is carried out at an ion implantation dose of from about 1E13 to about 1E14 atoms per square centimeter, and an ion implantation energy of from about 10 KeV to about 20 KeV.

44. A method according to claim 38, wherein said annealing step is at a temperature of about 800 to about 1000 degrees centigrade for a time period of about 10 to about 20 seconds.

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